Claims

I claim:

1. A method of fabricating a MOSFET comprising:

providing a semiconductor chip doped with impurity of a first conductivity type;

forming a first mask over the chip, the mask having openings which define the locations of first, second and third trenches, respectively;

etching the chip through the openings in the first mask to form the first, second and third trenches, thereby forming a first mesa between the first and second trenches and a second mesa between the second and third trenches;

forming an insulating layer on the walls of the trenches;

introducing a conductive gate material into the trenches;

forming a second mask covering the first mesa but having an opening over the second mesa;

introducing a first dopant of the first conductivity type through the opening in the second mask into the second mesa;

introducing a second dopant through the opening in the second mask into the second mesa, the second dopant being of a second conductivity type opposite to the first conductivity type and being introduced at a first energy level;

removing the second mask;

forming a third mask covering the second mesa but having an opening over the first mesa;

introducing a third dopant through the opening in the third mask into the first mesa, the third dopant being of the second conductivity type and being introduced with at a second energy level, the second energy level being greater than the first energy level; and

subjecting the chip to heat such that and the first, second and third dopants diffuse, the third dopant diffusing under the second trench, a junction between the first and second dopants forming a body-drain junction of the MOSFET.

2. The method of Claim 1 comprising introducing a fourth dopant of the first conductivity type into the first and second mesas, the fourth dopant forming a source region of the MOSFET.

3. The method of Claim 1 wherein introducing the second dopant comprises implanting boron.

4. The method of Claim 3 wherein introducing the third dopant comprises implanting boron.

5. The method of Claim 1 wherein subjecting the chip to heat causes a junction of the third dopant to meet a junction of the first dopant.

6. The method of Claim 5 wherein the junction of the third dopant meets the junction of the first dopant in a region adjacent a corner of the second trench.

7. The method of Claim 2 comprising forming a fourth mask having an opening over each mesa.

8. The method of Claim 7 comprising introducing a fifth dopant of the second conductivity type through the openings in the fourth mask to form body contact regions at the surface of the chip.

9. The method of Claim 7 comprising etching the chip through the openings in the fourth mask to form a groove in each mesa.

10. The method of Claim 9 comprising introducing a fifth dopant of the second conductivity type through the openings in the fourth mask to form a body contact region at the bottom of each groove.

11. The method of Claim 1 comprising:

forming a fourth mask having an opening over the first mesa;

implanting a fourth dopant of the first conductivity type at a third energy level through the opening in the fourth mask to form a first source region in the first mesa; and

forming a fifth mask having an opening over the second mesa; and

implanting a fifth dopant of the first conductivity type at a fourth energy level through the opening in the fifth mask to form a second source region in the second mesa, the third energy level being different from the fourth energy level.

12. A trench MOSFET comprising:

a semiconductor chip doped with impurity of a first conductivity type, the chip having first, second and third trenches formed at a surface of the chip, the first and second trenches defining a first mesa, the second and third trenches defining a second mesa;

a first source region of the first conductivity type in the first mesa, the first source region being adjacent the surface of the chip;

a second body region of a second conductivity type opposite to the first conductivity type in the first mesa, the second body region forming a first junction with the first source region, the second body region extending below the first and second trenches such that the second body region is adjacent the bottoms of the first and second trenches;

a third source region of the first conductivity type in the second mesa, the third source region being adjacent the surface of the chip;

a fourth body region of the second conductivity type in the second mesa, the fourth body region forming a second junction with the third source region, the fourth body region comprising a first channel region adjacent a wall of the second trench; and

a fifth drain region of the first conductivity type in the second mesa, the fifth drain region forming a third junction with the fourth body region.

13. The trench MOSFET of Claim 12 wherein the fourth body region comprises a second channel region adjacent a wall of the third trench.

14. The trench MOSFET of Claim 12 wherein the second trench has a first lower corner at a base of the first mesa and a second lower corner adjacent a base of the second mesa, the first body region wrapping around the first and second lower corners.

15. The trench MOSFET of Claim 14 wherein the first trench has a third lower corner and a fourth lower corner, the first body region wrapping around the third and fourth lower corners.

16. The trench MOSFET of Claim 12 wherein the fifth drain region is doped with impurity of the first conductivity type, a doping concentration of the fifth drain region being greater that a background doping concentration of the chip.

17. The trench MOSFET of Claim 12 comprising grooves at the top of the first and second mesas, respectively, and sixth body contact regions doped with impurity of the second conductivity type adjacent bottoms of the grooves.

18. The trench MOSFET of Claim 12 wherein the first source region extends downward from a surface of the chip a first distance and wherein the second source region extends downward from said surface of the chip a second distance, said first distance being greater than said second distance.